Amendments to the Claims:

Please amend claims 2-7, 19, 20, 22, 24-26, 29, 30, 32 and 34. Please cancel claims 1, 8-18, 21, 27, 28 and 35-43. Please add new claims 44-65.

The claims are as follows:

Listing of Claims:

1. (Canceled).

2. (Currently Amended The method of claim ~~1~~ 5, wherein said second width ~~is sub-minimum groundrule~~ has a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

3. (Currently Amended) The method of claim ~~1~~ 5, further including removing said patterned hard mask layer.

4. (Currently Amended) The method of claim ~~1~~ 5, wherein said patterned hard mask layer comprises silicon oxide.

5. (Currently Amended) A method of fabricating a polysilicon line, comprising:

forming a patterned hard mask layer over a polysilicon layer;

patterning the polysilicon layer to provide a hard mask-capped polysilicon line having a first width; and

isotropically removing portions of said polysilicon line to reduce said polysilicon line to a second width by

~~The method of claim 1, wherein isotropically removing portions of said polysilicon line~~ ~~comprises~~ converting a surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer.

6. (Currently Amended) The method of claim ~~1~~ 5, wherein the step of removing portions of the polysilicon line ~~comprises a treatment~~ includes oxidizing a surface of said polysilicon line in a saturated aqueous solution of O_3 to form said oxide layer on said polysilicon line followed by etching said oxide layer in a solution comprising ~~1 part 49%~~ HF in ~~50 to 300 parts of~~ water.

7. (Currently Amended) The method of claim ~~1~~ 5, wherein the step of removing portions of the polysilicon line ~~comprises a treatment~~ includes oxidizing a surface of said polysilicon line in a saturated aqueous solution of O_3 to form said oxide layer on said polysilicon line followed by etching said oxide layer in an HF containing vapor.

8. (Canceled)

9. - 18. (Canceled)

19. (Currently Amended) A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width; ~~and~~

isotropically removing portions of the polysilicon electrode to reduce said polysilicon line to a second width by converting a surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer; and

removing said patterned hard mask layer.

20. (Currently Amended) The method of claim 19, wherein said second width ~~is sub-minimum groundrule~~ has a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

21. (Canceled)

22. (Currently Amended) The method of claim 19, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon ~~gate~~ electrode and said patterned hard mask.

23. (Original) The method of claim 19, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

24. (Currently Amended) The method of claim 19, wherein said substrate is selected from the group consisting of silicon substrates, silicon on insulator substrates, gallium arsenide substrates and sapphire substrates.

25. (Currently Amended) The method of claim 19, wherein the step of removing portions of the polysilicon electrode ~~comprises a treatment~~ includes oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of O_3 to form said oxide layer on said polysilicon electrode followed by etching said oxide layer in a solution comprising ~~1 part 49%~~ HF in ~~50 to 300 parts of~~ water.

26. (Currently Amended) The method of claim 19, wherein the step of removing portions of the polysilicon electrode ~~comprises a treatment~~ includes oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of O_3 to form said oxide layer on said polysilicon electrode followed by etching said oxide layer in an HF containing vapor.

27. (Canceled)

28. (Canceled)

29. (Currently Amended) A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width;

measuring said first width;

comparing said first width to a target width and determining a ~~delta~~ differential between said first width and said target width;

calculating ~~an etch time or~~ a number of polysilicon oxidation/isotropic polysilicon oxide etch cycles based on said ~~delta~~ differential; and

~~performing an isotropic polysilicon etch for the calculated time or~~ performing the calculated number of polysilicon oxidation/isotropic polysilicon oxide etch cycles.

30. (Currently Amended) The method of claim 29, wherein said target width ~~is sub-minimum groundrule~~ has a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

31. (Original) The method of claim 29, further including removing said patterned hard mask layer.

32. (Currently Amended) The method of claim 29, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon ~~gate~~ electrode and said patterned hard mask.

33. (Original) The method of claim 29, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

34. (Currently Amended) The method of claim 29, wherein said substrate is selected from the group consisting of silicon substrates, silicon on insulator substrates, gallium arsenide substrates and sapphire substrates.

44. (New) A method of fabricating a polysilicon line, comprising:

forming a patterned hard mask layer over a polysilicon layer;

patterning the polysilicon layer to provide a hard mask-capped polysilicon line having a first width; and

isotropically removing portions of said polysilicon line to reduce said polysilicon line to a second width, said second width having a value less than a value of a minimum dimension producible by a photolithographic process used to form said patterned hard mask layer.

45. (New) The method of claim 44, further including removing said patterned hard mask layer.

46. (New) The method of claim 44, wherein said patterned hard mask layer comprises silicon oxide.

47. (New) The method of claim 44, wherein isotropically removing portions of said polysilicon line comprises converting a surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer.

48. (New) The method of claim 44, wherein the step of removing portions of the polysilicon line comprises oxidizing said polysilicon line in a saturated aqueous solution of O_3 to form an oxide layer on said polysilicon line followed by etching said oxide layer in a solution comprising HF in water.

49. (New) The method of claim 44, wherein the step of removing portions of the polysilicon line comprises oxidizing a surface of said polysilicon line in a saturated aqueous solution of O_3 to form an oxide layer on said polysilicon line followed by etching said oxide layer in an HF containing vapor.

50. (New) The method of claim 44, wherein the step of removing portions of the polysilicon line includes etching said polysilicon line in a solution of HF, HNO_3 and H_3PO_4 or includes etching said polysilicon in a solution of NH_4OH, H_2O_2 and water.

51. (New) A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width; and

isotropically removing portions of the polysilicon electrode to reduce said polysilicon electrode to a second width, said second with having a value less than a value of a minimum

dimension producible by a photolithographic process used to form said patterned hard mask layer.

52. (New) The method of claim 51, further including removing said patterned hard mask layer.

53. (New) The method of claim 51, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon electrode and said patterned hard mask.

54. (New) The method of claim 51, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

55. (New) The method of claim 51, wherein said substrate is selected from the group consisting of silicon substrates, silicon on insulator substrates, gallium arsenide substrates and sapphire substrates.

56. (New) The method of claim 51, wherein the step of removing portions of the polysilicon electrode comprises oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of O_3 to form an oxide layer on said polysilicon electrode followed by etching said oxide layer in a solution comprising HF in water.

57. (New) The method of claim 51, wherein the step of removing portions of the polysilicon electrode comprises oxidizing a surface of said polysilicon electrode in a saturated aqueous

solution of O_3 to form an oxide layer on said polysilicon electrode followed by etching said oxide layer in an HF containing vapor.

58. (New) The method of claim 19, wherein the step of removing portions of the polysilicon electrode includes etching said polysilicon electrode in a solution of HF, HNO_3 and H_3PO_4 or includes etching said polysilicon electrode in a solution of NH_4OH, H_2O_2 and water.

59. (New) A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width; and

isotropically removing portions of the polysilicon electrode to reduce said polysilicon electrode to a second width;

removing said patterned hard mask layer; and

forming source/drain regions in said substrate after removing said patterned hard mask layer.

60. (New) The method of claim 59, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon electrode and said patterned hard mask.

61.The method of claim 59, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

62. (New) The method of claim 59, wherein said substrate is selected from the group consisting of silicon substrates, silicon on insulator substrates, gallium arsenide substrates and sapphire substrates.

63. (New) The method of claim 59, wherein the step of removing portions of the polysilicon electrode comprises oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of O_3 to form an oxide layer on said polysilicon electrode followed by etching said oxide layer in a solution comprising HF in water.

64. (New) The method of claim 59, wherein the step of removing portions of the polysilicon electrode comprises oxidizing a surface of said polysilicon electrode in a saturated aqueous solution of O_3 to form an oxide layer on said polysilicon electrode followed by etching said oxide layer in an HF containing vapor.

65. (New) The method of claim 59, wherein the step of removing portions of the polysilicon electrode includes etching said polysilicon electrode in a solution of HF, HNO_3 and H_3PO_4 or includes etching said polysilicon electrode in a solution of NH_4OH, H_2O_2 and water.